REMARKS

The Examiner rejects Claims 8, 10 and 14-15 under 35 U.S.C. §103(a) as being unpatentable over Palmer, Jr., et al in view of Hyatt. The Examiner states with regard to Claim 8, Palmer, Jr., et al discloses an integrated circuit computer system shown in Figure 2, item 6i having a processor interconnected with memory shown in Figure 1, item 6d and peripheral circuits on the integrated circuit, Figure 1, items 6f, 6c and 6a coupled to a security system. With regard to Claim 14, Examiner states that the reference shows a security system for integrated circuit computer system for applying a plurality of commands to a plurality of ports for the processor and refers to Figure 1, items 6a, the block labeled PROCESS CONTROL PROGRAM, item 4, item 6f, a program stored in a memory coupled to the processor to process to a plurality of commands to produce a password shown in Figure 2, items 6i, 6c and comparing the produced password with a predetermined password shown in Figure 1, item 6 and Figure 2, item 6i.

The Examiner states that Palmer, Jr., et al does not specifically disclose the use of a single chip and that Hyatt discloses a single chip integrated circuit. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at a time of the invention to modify the references to include the use of a single chip for the reasons provided Hyatt in Column 1, Lines 48-58, Column 5, Lines 54 to Column 6, Line 34.

The fact that this rejection has now been modified from an '102 Rejection to an '103 Rejection, does not change the fact that the Examiner's analysis of Palmer, Jr. et al is incorrect.

First of all, it must still be noted that, referring to the brief description of the figures in Palmer, Jr., et al., Figure 1 is not a block diagram for the system, but is a flow diagram for the data in the system. The Examiner's first error is to assume that items 6b, 6d and 6e are inputs to the processor which he is obviously reading on the process control program (unlabeled in Figure 1). Figure 2 is a block diagram of the system. It is clearly

shown in Figure 2 that items such as the operating system program, the look-up table and constants' table are stored in the 1024 byte ROM and the software clock and parameter storage are stored in the 64 byte RAM. Thus, they are not inputs to the signal chip microcomputer which is clearly shown as item 6i and contains the ROM and RAM memories. Referring to Figure 2, element 6i is referred to as "single chip microcomputer", which indicates that item 6i is a single integrated circuit. The peripheral circuit which the Examiner states are integrated on the chip are the appliance access control unit 6f, which is clearly shown as a separate device and the optical card reader 6c. Those skilled in the art know that an optical card reader cannot be integrated onto an integrated circuit chip. Furthermore, the clock and data outputs of the optical card reader 6c are applied to the test inputs T0 and T1, respectively of the single chip microcomputer, which indicates that they are outside of the integrated circuit chip and thus do not meet the requirements of Claim 8.

Figure 3 is a schematic diagram of the access control module, as clearly shown from the brief description of the figures, a typographical error in column 2, line 55 referring to Figure 2, notwithstanding. In Figure 3 there is a single data input bus shown as pins 1-9 of connector J2 for conveying signals data 0 through data 7 and strobe bar to the microcomputer U2. The optical card, which is an external device, is coupled to the microcomputer U2 via test terminals T0 and T1.

The Examiner refers to items 6c and 4. These items are the card reader 4 and the card reader portion of the access control module 6, respectively. Referring now to Figure 2 of the cited reference, the optical card reader 6c is coupled to the single chip microcomputer 6i via a clock line and a data line which forms a first port. The password entered via the optical card reader is compared with a password stored in the ROM of the single chip microcomputer, which is internal to the microcomputer, as clearly shown in Figure 2, and discussed above. Accordingly, applying this reference to the present invention, the "command" would be applied to the test port T0, T1; would be read by the single chip microcomputer and compared to a password stored in its memory. There is no showing of the password being generated by a plurality of commands applied to a plurality of ports for the processor. Just to make sure that the concept of "port" is clear,

applicants previously submitted a portion of the text "Imbedded Microprocessor Systems - Real World Design" by Stuart R. Ball. Furthermore, applicants had previously submitted a copy of a portion of the text "Programming Embedded Systems I" by Michael J. Paunt which clearly shows on page 1-12 that standard 8051s (microprocessors) have four 8-bit ports, all the ports being bidirectional. Therefore, it should be clear that a "port" is a group of I/O pins on a microcomputer chip which operate together for a particular function.

Thus, the fact that the store computer system inputs a "seed" into the access control module of the cited reference is irrelevant here because the seed and the clock output are used to find the password stored in the computer which is compared to the input password. Therefore, even if one were to ignore the arguments above and characterize the seed as a second command, it would not anticipate the present invention or render it obvious because it is not used to generate the password, which is read by the optical card reader.

The Examiner's citing of the Hyatt reference does not help this cause. Although Hyatt discloses a single chip computer architecture, that is clearly not the only difference between the present invention and the Palmer, Jr. et al reference, the Examiner's statements to the contrary notwithstanding. In fact, it is not clear that Hyatt adds anything to the Examiner's argument at all. In Hyatt, at Column 8, Lines 35-46, it recites that the date processor contains an integrated memory to provide a complete integrated circuit computer which might be called a monolithic computer. It further recites that the monolithic data processor can be implemented on a single integrated circuit chip which includes a read only memory, an alterable memory and a program execution circuitry all in the same chip. That much is shown in Palmer, Jr. et al by element 6l which is clearly labeled "single chip microcomputer". What Palmer, Jr. et al does not show is the peripherals being on chip, since optical card readers and the like are clearly are not on chip and Palmer, Jr. et al. Hyatt describes peripherals such as the photo electric tape reader in Column 8, Line 56 *et seq*, as specifically refers to a particular punch tape reader at Column 10, Lines 41-45. As will be clearly well known

to those skilled in the art, these tape readers are not on the chip and, therefore, the recitation of Hyatt really adds nothing to the Examiner's argument, the Examiner's statements to the contrary notwithstanding.

Furthermore, in the Examiner's response to arguments, in Paragraph 45 of the Official Action, the Examiner recites that Applicant's appear to be reading in definitions which are not reflected in the claims. The Examiner states that we should change the claims in order to reflect the definition of a term of art. That is not a law. Applicant's are clearly entitled to use terms of art and the terms of art should be given their ordinary meaning as would be understood by those skilled in the art. Applicant's are not required to amend the claims in this respect, and, given the negative implications of claim amendments, Applicant's decline to do so. However, the Examiner must use the known definition of terms of art and not apply his own definitions thereto. If the Examiner disagrees with the definitions we have supplied in the past, the Examiner is requested to either cite a reference as a basis for that rejection or supply an affidavit in accordance with the MPEP 2144.03.

The Examiner complained in Paragraph 46 of the Official Action that Applicant's provided abstract hypothetical arguments relating to "reversed situations" which the Examiner declined to respond to. The purpose of those hypothetical arguments was to show that, even if the inputs were reversed, they still did not anticipate or render the present invention obvious. Although, the Examiner will undoubtedly will not respond to this argument, Applicants would like to keep this argument on the record and therefore have maintained the following discussion:

> Although the Examiner has not specifically discussed the possibility, even if one were to reverse the situation in which the seed were read in through the optical card reader and the password came in through the main computer interface port, the situation would not change, because the information coming through the main computer interface port is a "seed" which is combined with an output of the clock to produce a pointer to the password. The hardware system clock and

software clock are both shown in Figure 2 as being internal to the single chip microcomputer 6i and thus do not come from a second port.

In view of the fact that Claim 8 recites applying a plurality of commands to a plurality of ports and having the program operating the processor or being operable to control the processor to process the plurality of commands to produce a password, Claim 8 is clearly distinguished from this reference. Claim 14 recites "means for applying a plurality of commands to a plurality of ports for a processor of said system "which is not shown or suggested by Palmer, Jr., et al. Claim 10 recites that the processor in Claim 8 receives the plurality of commands which are applied to a plurality of ports in a specific time sequence. This additional feature is not shown or suggested by Palmer, Jr., et al. and provides a significant improvement by making the code more secure without the need for additional circuitry. Similarly Claim15, which is dependant on Claim 14, recites this same feature and is therefore separately patentably distinct from Palmer, Jr., et al.

The Examiner rejects Claims 8, 10 and 14-15 under 35 U.S.C. 103(a) as being unpatentable over Angelo in view of Hyatt. The Examiner states that Angelo discloses a method for enabling power to all portions of a computer system based upon the results of a two-piece user verification process that is completed as part of a secure power-up procedure. The Examiner specifically highlights portions of the text which recites that at some point during the secure power-up procedure, the computer user provides an external token or smart card that is coupled to the computer using specialized hardware and that the computer user is required to enter a plain text user password or, a password generated by the aid of biometrics.

The Examiner states that the applied references do not expressly disclose the use of a single chip and that Hyatt discloses a single chip integrated circuit. The

Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the references to include the use of a single chip for the reasons discussed in the above rejection.

This rejection is respectfully traversed. First of all, the system described in Angelo at col. 3, lines 48-58 includes bay door/case locks and mass data storage devices. The system provides security by withholding power to the peripheral devices and to the bay door/case locks forcing the possessor of a stolen computer to physically damage the computer casing. Accordingly, this reference is not applicable to the present invention, where such devices can not exist. Furthermore, the two-piece nature of the authorization process, does not require utilization of applying commands to two input ports on a processor. In fact, referring to Figure 1, we see that the floppy/keyboard controller 136 has coupled thereto a keyboard 159 via keyboard connector 158 and a probe 186, into which the token 188 is plugged, is coupled to the floppy/keyboard controller 136 via an RS-232 connector 146 and a com port adapter 184. Accordingly, both of the inputs into the system that are required, that is, the token and the typed in password, pass through the floppy/keyboard controller 136 and via a single bus into the port comprising lines 106 and 108.

As stated above, Hyatt fails to show or suggest utilization of peripherals on – chip. In addition, Hyatt fails to show the utilization of applying a plurality of commands to plurality of ports in order to generate a password. In view of the fact that Angelo passes all of its signals through a single port, the combination of these references teaches away from the present invention .

Accordingly, these references, either singly or in combination fail to show or suggest the application of a plurality of commands to a plurality of ports for generating a password, as required in Claim 8. Nor do they show or suggest the "means for applying a plurality of commands to a plurality of ports of said system "required by Claim 14.

Claim 10 recites that the processor in Claim 8 receives the plurality of commands which are applied to a plurality of ports in a specific time sequence. This additional feature is

not shown or suggested by Palmer, Jr., et al. and provides a significant improvement by making the code more secure without the need for additional circuitry. Similarly Claim15, which is dependant on Claim 14, recites this same feature and is therefore separately patentably distinct from Palmer, Jr., et al.

The Examiner rejects Claims 4, 5, 9, and 15 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Hyatt and further in view of Raghavachari. The Examiner states that Palmer, Jr. et al does not expressly disclose the use of a single chip and this is disclosed in Hyatt or disclose a scan-path interface circuit for reading out a predetermined memory or register in the system and that this is disclosed in Raghavachari. The Examiner concludes that it would have been obvious to one of ordinary skill in art at the time the invention was made to combine the three references.

This rejection is respectfully traversed. First of all, the discussion above concerning Palmer, Jr. et al applies here and Claim 4 clearly requires a plurality of commands applied to a plurality of input ports on a processor to process the commands to produce a password, which is not shown by Palmer, Jr. et al.

The Hyatt reference has also been discussed above in connection with its combination with Palmer, Jr. et al and that argument applies here as well.

Furthermore, with regards to Raghavachari, Figure 1 clearly shows that all input to the system comes through the port comprising lines TCK, TMS and TDI. These lines come through the boundary scan-port and control 15. No other input lines are shown. Therefore, these lines comprise the only input port to the device. Accordingly, this reference can not show or suggest the application of a plurality of commands to a plurality of input ports and processed to generate a password, as required by Claim 4. In fact, since both references show the utilization of a single port, the combination teaches away from the present invention.

The Examiner states that with regard to Claim 9, Palmer, Jr. et al does not expressly disclose a switching circuit coupled to the scan-path interface. The Examiner states that Raghavachari discloses that many integrated circuits are accessed via scan-

ports and specifically discloses a switching circuit coupled to the scan-path interface. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Palmer, Jr. et al with Raghavachari.

Assuming, arguendo, that Palmer, Jr. et al, Hyatt and Raghavachari were to be combined, this still would not teach the utilization of applying commands to a plurality of ports to be processed into a password because Raghavachari only shows a single input port and Palmer, Jr. et al., which does show two input ports, shows them each being used for separate purposes. Accordingly, even if these two devices could be combined, it would not yield the present invention or suggest the present invention.

The Examiner states with regard to Claim 5, the Palmer, Jr. et al reference inherently discloses a specified time sequence.

The "sequence" of Palmer, Jr. et al would that the input through main computer interface 6a would have to occur at a time previous to the input to card reader 4, 6c. However, the reference fails to show or suggest the application of a plurality of commands applied to a plurality of input ports in a specific time sequence to be processed into a password, as would be required by the combination of Claims 4 and 5.

Claim 15 recites that the processor receives a plurality of commands which are applied to the plurality of ports in a specific time sequence. As discussed above, the combination of the three references fails to show or suggest the use of a plurality of ports and therefore Claim 15 is patentably distinct from this combination of references.

The Examiner rejects Claims 6, 7, 11, 12, 13, 16, 17, 19, 20 and 21 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Hyatt and Raghavachari and further in view of Jacobson, et al. These claims are dependent upon Claims 4, 8 or 14, the patentability of which has been discussed above. These claims are patentable for the same reasons.

The Examiner rejects Claim 18 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Hyatt and further in view of Jacobson, et al. Claim 18 is dependent upon Claim 14. The patentability of Claim 14 over the Palmer, Jr. et al reference having been discussed above, Claim 18 is patentable for the same reasons.

The Examiner rejects Claims 4-7, 9, 11-13 and 16-21 under U.S.C. 103(a) as being unpatentable over Angelo in view of Hyatt and further in view of Bianco, et al. The Examiner states that Angelo discloses a method for enabling power to all or portions of a computer system based on the results of a 2-piece user verification process that is completed as part of a secure power-up procedure. The Examiner states that Angelo does not expressly disclose a scan-pass interface circuit for comparison for a predetermined memory or register and a switching circuit is responsive to the comparison. The Examiner states that Bianco, et al. discloses a set/scan test capability which is provided for a circuit that includes sensitive subcircuits that can be latched out to prevent reverse engineering of the sensitive elements. The Examiner states that Hyatt discloses a single chip integrated circuit. The Examiner concludes that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Angelo reference with Hyatt and with the Bianco, et al. reference.

This rejection is respectfully traversed. The Angelo reference has been discussed above in connection with the rejection of Claims 8, 10 and 14-15. As stated above, Angelo specifically shows all of the inputs needed to generate the password coming through a single input port to the processor. With respect to Bianco, et al, the Examiner specifically points to Figure 6. Figure 6 does show a CPU connected to a system to protect sensitive information from a data scan. However, reading the remainder of the reference, it is clear the protection is provided by an encryption program stored in EEPROM 58. Once the device has been tested by the manufacturer, the system is programmed to bypass the data stored in the sensitive area unless a code equal to that stored in the EEPROM is applied. There is nothing in this reference that shows or even suggests the application of a plurality of commands to a plurality of ports

for the processor 50 to be processed into a password. The password goes through the S/S control 14. Furthermore, the system of Bianco, et al requires considerable additional circuitry to that of the present invention. In fact, the elegance of the present invention is that no additional circuitry is required, it utilizes attributes of the microprocessor that are already present to provide the additional security. Combining these references with Hyatt does not overcome the distinctions of the present invention over the combination for the reasons discussed above. Therefore, these references singly, or in combination do not show or suggest the present invention. Accordingly, the present claims already clearly distinguished from these references either singly or in combination.

Claim 4 specifically recites that the security mechanism receives a plurality of commands applied to a plurality of input ports which are processed to produce a password, which is not shown or suggested by the combination of references. Claim 11 is dependent from Claim 8 which also recites that the processor receives a plurality of commands at a plurality of input ports which are processed to produce a password. Claim 12 is also indirectly dependant from Claim 8 and is therefore patentable for the same reasons. Claim 13 is dependant from Claim 10 which adds that the receipt of the plurality of commands applied to the plurality of ports is in a specific time sequence. Claim 13 is therefore patentably distinct from the combination of references. Claim 16 is dependant form Claim 14 which recites means for applying a plurality of commands to a plurality of ports and a program stored in memory coupled to the processor for processing the commands to produce a password. It is therefore patentably distinct from the combination of references. Claim 17 is dependent form Claim 15 which recites that the plurality of commands are applied to the plurality of ports in a specific time sequence. Claim 17 is therefore patentably distinct from the combination of references. Claim 18 is dependent from Claim 14 which recites means for applying a plurality of commands to a plurality of ports for a processor and a program stored in memory coupled to the processor which processes the commands to produce a password and is therefore patentably distinct. Claims 19-21 are dependant from Claims 15-17, respectively and are therefore patentable for the same reasons.

Accordingly, Applicants believe that the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

Texas Instruments Incorporated

By _____

William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
(972) 917-5452